ABSTRACT OF THE DISCLOSURE

To provide a variable dividing circuit having a high operational speed. The variable dividing circuit includes a shift register configured by cascade connection of D-type flip-flops (D11, D12, …, D1n) with an initializing means by clock synchronization; and a multiplexer 12 for selecting any one of output signals at respective stages of the shift register; wherein the variable dividing circuit initializes each stage of the D-type flip-flops. In this case, in an input terminal 10 of the flip-flop at the first stage, a signal at an H level or at an L level is inputted in accordance with an initializing means.